# Worksheet 1 Internal computer architecture Answers

# Task 1 Input – process - output

Complete the diagrams below outlining the basic operations of various computer systems

1. Writing a story using a word processing package

Process

Keyboard presses

Characters encoded

Story displayed

Input

Output

Input

Position on map displayed

Coordinates matched to place on map

GPS signal

Input

Image displayed

Image digitised

Image through lens, button press

Input

Validated ticket

Amount paid checked against time of stay

Ticket, money

1. Showing the position of a car on a Sat Nav

Process

Output

1. Taking a photo on a Smartphone

Process

Output

1. Paying for a car park ticket in an automated machine

Process

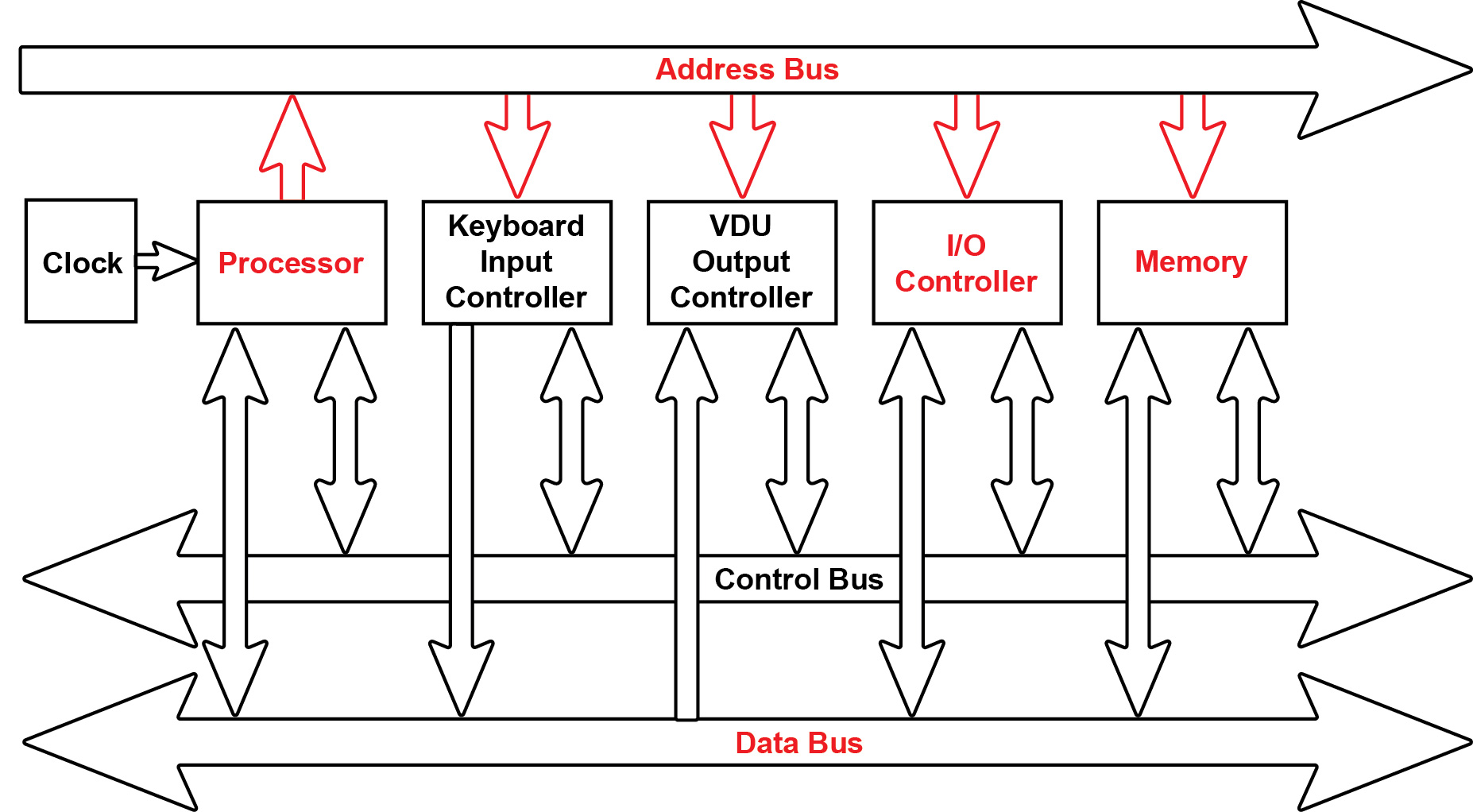
Output

**Task 2 System buses**

Data within a computer is moved around its various components using a series of interconnections known as the system bus.

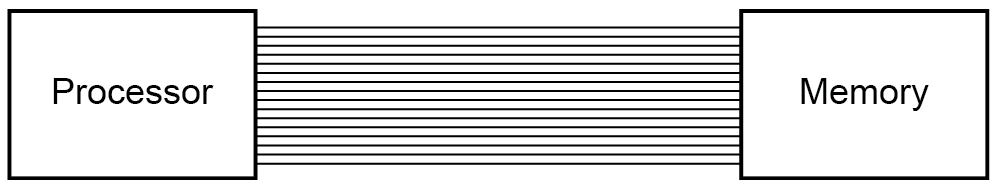
Complete the diagram below to label the following parts showing the direction in which addresses travel:

**Processor, Data bus, Address bus, I/O controller, Main memory**



**Task 3 Word length**

Memory is divided into equal units called **words**. Each word has a separate memory address.



A processor uses a word length of 16 bits and has an address bus of 16 lines.

1. What is the maximum number of addressable words in memory? 216 = 65,536
2. What is the overall memory capacity in KiB? 65,536 x 2 bytes (16 bits) / 1024 = 128 KiB
3. How does the width of the address bus affect system performance? Increases the number of addressable memory spaces available // Increases the maximum amount of primary storage. This indirectly affects system performance if large data files (e.g. image files) need to be manipulated or large programs executed. Also multi-processing will be more efficient as many processes can be held simultaneously in memory.
4. How does the width of the data bus affect system performance? Increases the data transfer rate // number of bits that can be transferred at one time, therefore increases system performance.

**Task 4 Memory and the stored program concept**

Using standard von Neumann architecture, instructions and data both share the same memory space.

|  |  |
| --- | --- |
| **Memory** | |
| **Address** | **Instruction / Data** |
| 0 | 10010111 00101111 |
| 1 |  |
| 2 | 00000000 11010100 |
| … | … |
| 255 | 00000000 01001010 |

One problem with this model is that the CPU can either be reading an instruction or reading/writing data to or from memory, but not both at the same time since instructions and data use the same bus system, which is a performance limitation.

1. Name another architecture that resolves this issue. How does it differ from von Neumann architecture?

Harvard architecture – this has separate memories for instructions and data. Separate data buses transfer instructions and data to and from memory

1. What other advantages are there of using this architecture?

Avoids data erroneously overwriting programming instructions in the same address location;

Data cannot be executed as code;

Can employ larger data or instruction memory as required // memory address structures do not need to be the same;

Data and instructions can have different word lengths;