# Homework 2 Adders and D-type flip-flops Answers

1. (a) What is a **half adder**? [3]

 It is a logic circuit which takes an input of 2 bits; and outputs the sum; and the carry.

 (b) Complete the diagram below to construct a half adder circuit. [2]

 Answer:



(c) Draw the truth table for the half adder, which has inputs A and B and
outputs S and C. [2]

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **A** |  | **B** |  | **S** | **C** |
| 0 | + | 0 | = | 0 | 0 |
| 0 | + | 1 | = | 1 | 0 |
| 1 | + | 0 | = | 1 | 0 |
| 1 | + | 1 | = | 0 | 1 |

 (d) What are the inputs to a full adder? [2]

 Two input bits A and B; and the carry bit from a previous addition.

 (e) Show the outputs S0, S1, S2, S3, C1, C2, C3 from the following 4-bit adder. [4]

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | **0** C3 | **1** C2 | **1** C1 | **0** C0 |  |
|  | 1 A3 | 0 A2 | 1 A1 | 1 A0 |  |
| + | 0 B3 | 0 B2 | 1 B1 | 1 B0 |  |
| = | **1** S3 | **1** S2 | **1** S1 | **0** S0 |  |

2. (a) What is an edge-triggered D type flip-flop? [3]

 A flip flop is an elemental sequential logic circuit; that can store one bit; for the duration of a clock pulse; and flip between two states 0 and 1.

 (b) Draw the flip flop’s output Q on the graph. [4]

Answer: Allow one mark where Q = D on each rising clock edge.



 [Total 20 marks]