# Worksheet 2B The Processor Answers

1. A computer is designed to be programmed using simplified assembly language. The instruction in memory location **020** is **SUB R1, R0, 101** and is used to subtract the value stored in memory location **101** from the value stored in the General Purpose Register **R0** and store the result in **R1**.

Numerical values are being used and are labelled with a # mark. The value currently in **R0** is **#40**. There is a value of **#15** in memory location **101**.

Complete the diagrams of the states of the processor components at various stages in the Fetch-Execute cycles showing how the result of this instruction is determined and stored in **R1**. Also add to the diagram a description of what is happening at each part of the three main stages, (the first has been completed as an example): **Fetch – Stage 1**



**Description of diagram:**

*The Program Counter contains the memory address of the next instruction to be processed, (020). This is copied into the Memory Address Register so that the instruction can be read. The memory location is requested to be read by the process.*

 **Fetch – Stage 2**



**Description of diagram:**

*The instruction stored in address 020 is placed on the data bus and read into the Memory Buffer Register and the Program Counter is incremented by 1.*

**Fetch – Stage 3**



**Description of diagram:**

*This instruction is copied from the Memory Buffer Register into the Current Instruction Register.*

 **Decode – Stage 4**



**Description of diagram:**

*The instruction in the CIR is decoded by the Control Unit. Operands in memory are required so the address of the operand is copied into the MAR. The data stored in address 101 is placed on the data bus and read into the Memory Buffer Register.*

**Execute – Stage 5**



**Description of diagram:**

*The values read into the processor are passed to the ALU to perform the subtraction. The result of the instruction is stored back into R1.*

1. The next instruction at address **021** is **STR R1, 102** where the result of the previous instruction is written to memory. Describe broadly the process the Fetch-Execute cycle will follow to achieve this.

The stages are:
* Instruction fetched from memory location
* Stored in the CIR
* PC incremented by one
* Instruction decoded by the Control Unit
* Value in R1 copied to MBR
* Address (102) from instruction used by MAR
* Value written to memory location 102