# Worksheet 2 Adders and D-type flip-flops

**Task 1**

1. (a) Complete the truth tables below for the AND gate and the XOR gate.

|  |  |  |
| --- | --- | --- |
| **Input A** | **Input B** | **A · B** |
| 0 | 0 |  |
| 0 | 1 |  |
| 1 | 0 |  |
| 1 | 1 |  |

|  |  |  |
| --- | --- | --- |
| **Input A** | **Input B** | **A ⊕ B** |
| 0 | 0 |  |
| 0 | 1 |  |
| 1 | 0 |  |
| 1 | 1 |  |

*AND gate* *XOR gate*

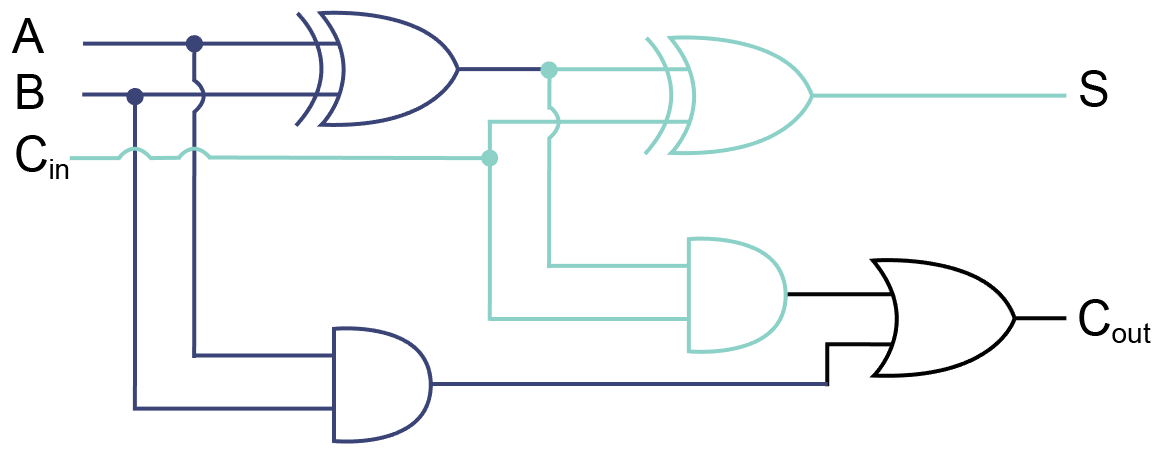
(b) Draw a circuit corresponding to S = A ⊕ B

(c) Draw a circuit corresponding to C = A **·** B

(d) Combine these two circuits to form a half-adder which has inputs A and B out outputs S and C.

(e) What do the outputs S and C represent?

2. (a) Below is a logic circuit for a full adder.



What are the inputs to a full adder?

Write the Boolean expressions for S and Cout representing this logic circuit.

(b) Show the outputs S0, S1, S2, S3, C1, C2, C3 from the following concatenated adders.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | C3 | C2 | C1 | C0 |  |
|  | 0 A3 | 1 A2 | 1 A1 | 1A0 |  |
| + | 0 B3 | 1 B2 | 0 B1 | 0 B0 |  |
| = | S3 | S2 | S1 | S0 |  |

3. Complete the following truth table for a full adder.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **A** |  | **B** |  | **Cin** |  | **S** | **Cout** |
| 0 | + | 0 | + | 0 | = |  |  |
| 0 | + | 0 | + | 1 | = |  |  |
| 0 | + | 1 | + | 0 | = |  |  |
| 0 | + | 1 | + | 1 | = |  |  |
| 1 | + | 0 | + | 0 | = |  |  |
| 1 | + | 0 | + | 1 | = |  |  |
| 1 | + | 1 | + | 0 | = |  |  |
| 1 | + | 1 | + | 1 | = |  |  |

**Task 2**

5. (a) What are the characteristics of an edge-triggered D-type flip flop?

(b) What is a D-type flip flop used for?

(c) Draw the flip flop’s output Q on the graph.

