**Fetch Decode Execute Cycle**

Textbook link: [Proquest eBook Page 277](https://ebookcentral.proquest.com/lib/godalming-ebooks/reader.action?docID=2131082&ppg=286)

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| **Phase** | **Step** | **Description** |
| Fetch | 1 | Program Counter (PC) set to Main Memory address of first Instruction |
|  |  | PC content (the address) copied to Main Memory Address Register (MAR) |
|  |  | Address Bus is used to transfer this address to Main Memory |
|  | 2 | Content of addressed Main Memory location moved into the Memory Buffer Register (MBR) |
|  |  | Data Bus is used to transfer this content to the MBR |
|  | 3 | Program Counter is increment |
|  | 4 | Instruction in MBR is copied to the Current Instruction Register (CIR) |
| Decode | 5 | The Instruction in CIR is decoded by the Control Unit |
|  |  | Instruction is split into Opcode and Operand |
| Execute | 6 | Data is fetched if instruction includes memory address (using MAR and MBR) |
|  |  | The opcode identifies the instruction to execute / operation to perform |
|  |  | The instruction is executed by the relevant part of the processor (e.g. ALU) |
|  |  | The result may be stored in accumulator, registers, main memory, depending on operation |

Sometimes called the Fetch Execute cycle, in which case the Decode phase is considered to be the first step of a 2-step Execute phase.