1 A burglar alarm system is to be implemented that has the following sensors:

- a door sensor **D** that outputs TRUE when the door is open and FALSE when the door is shut
- a pressure mat sensor **M** that outputs TRUE while a weight is detected on it and FALSE when no weight is detected on it.

The alarm also has a key **K** that turns the alarm on and off. **K** outputs a TRUE signal when the alarm is switched on and FALSE when the alarm is off.

The alarm output **A** sounds a bell. It should be TRUE if:

- the alarm is on AND
- either of the sensors **D** or **M** are set to the value TRUE.

(a) In the space below, draw a logic circuit that will behave as described above for the inputs **D**, **M** and **K** and the output **A**.

(2)

(b) Write a Boolean expression to represent the logic of this alarm system.

A=.....

(2)

(c) In this alarm system, the alarm bell will sound only while the door is open or a weight is placed on the pressure mat. If someone who has stepped on to the mat moves off it, or an open door is closed, the alarm bell will stop ringing.

A D-type flip-flop could be incorporated into the logic circuit so that the alarm bell would continue to sound after a person closed the door or moved off the pressure mat.

Explain how this could be achieved. In your answer refer to:

- why a D-type flip-flop would be suitable for this task
- where the D-type flip-flop would need to be inserted into the circuit
- what additional input the D-type flip-flop would need.

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(3)
(Total 7 marks)

2 (a) Complete the truth table below for a NAND gate.

NAND gate		
Input A	**Input B**	**Output**
0	0	
0	1	
1	0	
1	1	

(1)

(b) Multiplexors are used in electronic switching.

A 2-to-1 multiplexor has a Boolean equation where A and B are two inputs, S is the selector input, and Q is the output.

$$Q = (A.\overline{S}) + (B.S)$$

(i) Complete the truth table for the above Boolean equation.

S	A	B	$\overline{S}$	$A.\overline{S}$	B.S	Q
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				

(3)

(ii) Draw a circuit for the Boolean equation in the rectangle below.

(4)

(iii) By considering its inputs and outputs, describe what the 2-to-1 multiplexor circuit does.

.....

.....

.....

(1)
(Total 9 marks)

3 (a) Complete the truth tables for the following logic gates.

OR gate

Input A	Input B	Output
0	0	
0	1	
1	0	
1	1	

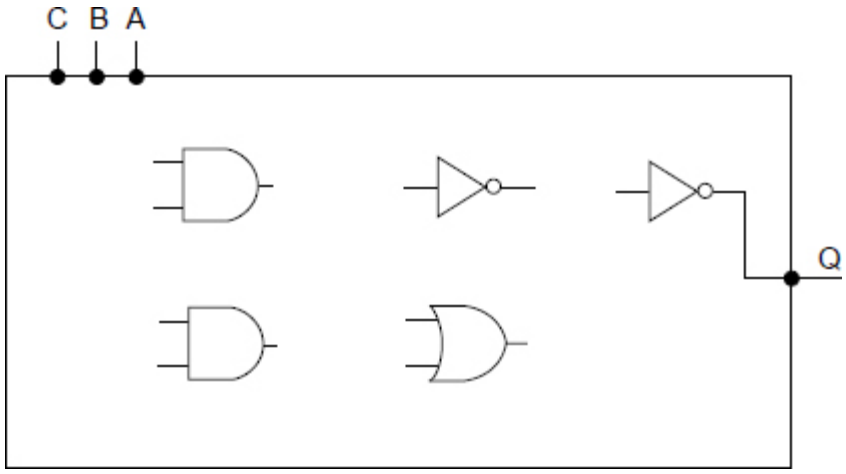
NAND gate

Input A	Input B	Output
0	0	
0	1	
1	0	
1	1	

(2)

(b) Represent the following Boolean equation as a logic circuit by completing the diagram below.

$$Q = \overline{\overline{A \cdot \overline{B}} + B \cdot C}$$



(5)

(c) Simplify the following expression.

$$\overline{\overline{A} + \overline{B}} + B \cdot \overline{A}$$

Show each stage of your working in the space below.

(2)

Final answer .....

(1)
(Total 10 marks)

4

(a) State the names of the logic gates represented by each of the three truth tables below.

Input A	Input B	Output
0	0	0
0	1	0
1	0	0
1	1	1

Logic gate name .....

Input A	Input B	Output
0	0	1
0	1	0
1	0	0
1	1	0

Logic gate name .....

Input A	Input B	Output
0	0	0
0	1	1
1	0	1
1	1	0

Logic gate name .....

(3)

(b) Simplify the following Boolean expressions.

(i) B . (A+$\bar{A}$)

.....

.....

(1)

(ii) A . B + B

.....

.....

(1)

(iii) $\overline{B} \cdot (\overline{\overline{A}+\overline{B}})$

.....

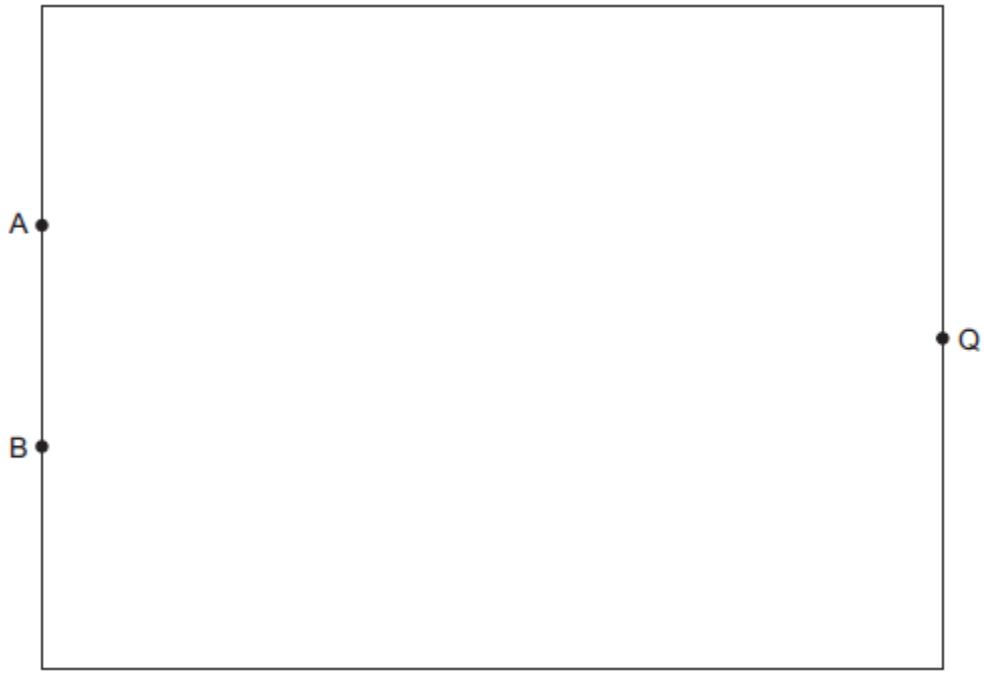
.....

(2)

(c) Draw a logic circuit for the following Boolean expression:

$$Q = (A \oplus B) \cdot B$$

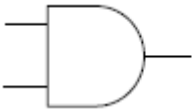
You will need to make use of the symbols below when drawing your logic circuit.



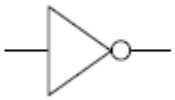
(2)
(Total 9 marks)

5

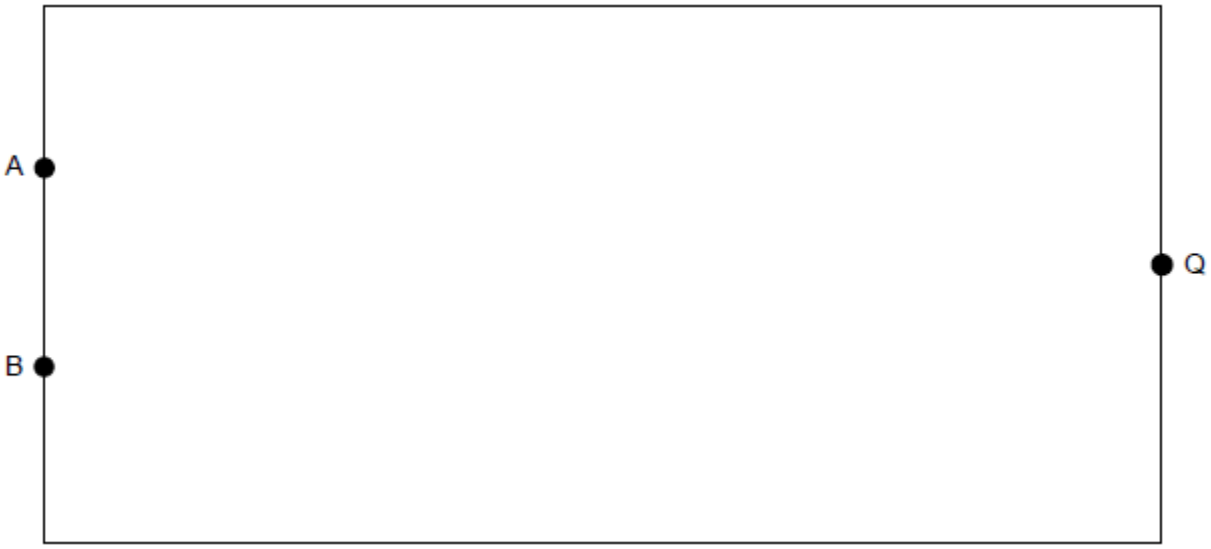
(a) Represent the Boolean equation Q = $\overline{\overline{A}.\overline{B}}$ as a logic circuit by drawing a diagram in the space below using **only** the following symbols:



AND



NOT



(3)

(b) Use the following truth tables to demonstrate that A + B = $\overline{\overline{A}.\overline{B}}$

A	B	A + B
0	0	
0	1	
1	0	
1	1	

A	B	$\overline{A}$	$\overline{B}$	$\overline{A}.\overline{B}$	$\overline{\overline{A}.\overline{B}}$
0	0				
0	1				
1	0				
1	1				

(4)

(c) What is the name commonly associated with the statement A + B = $\overline{\overline{A}.\overline{B}}$?

.....

(1)

(d) Simplify the Boolean expression below.

$$A.B.\overline{C} + A.\overline{C}$$

Show each stage of your working in the space below.

(2)

Final answer .....

(1)
(Total 11 marks)

6

(a) Complete the truth tables for the following logic gates.

AND Gate		
Input X	**Input Y**	**Input Q**
0	0	
0	1	
1	0	
1	1	

XOR Gate		
Output X	**Input Y**	**Output Q**
0	0	
0	1	
1	0	
1	1	

(2)

(b) A line-following robot has three sensors. It moves along a black line on a white background whilst the following conditions are met:

- the ultrasonic sensor U does not detect any obstacle
- either, but not both, of the infrared sensors L and R are on the black line.

Sensor U returns 1 if it detects an obstacle and 0 if the path is clear.
Sensors L and R each return 1 if they detect black and 0 if they detect white.

A logic circuit will process the input from the sensors and produce an output M.

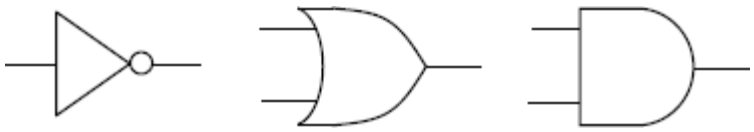
M should be 1 if the robot is to move and 0 if the robot should stop.

(i) Represent the output M as a Boolean expression.

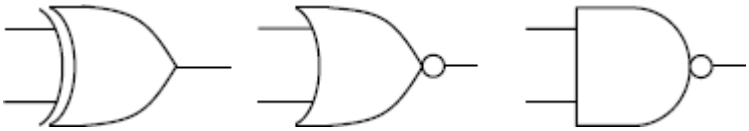
M = ...

(3)

(ii) The following symbols are used to represent logic gates:



NOT OR AND



XOR NOR NAND

Using a combination of any of the above logic gates draw a logic circuit for this system in the box below. You will **not** need to use all of the different types of logic gates.

(3)

(c) Apply De Morgan's Law(s) to the following expression and simplify the result.

$Q = \overline{\overline{A} + (B \cdot A)}$

Show the stages of your working.

.....

.....

.....

.....

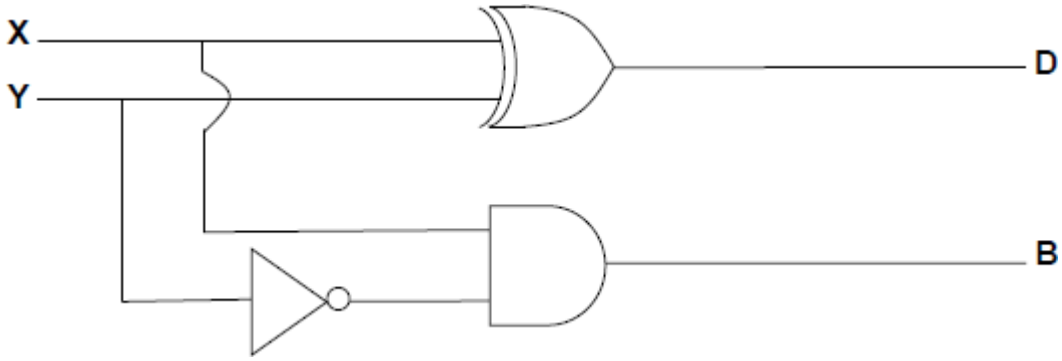
(2)

Final answer .....

(1)

(Total 11 marks)

7 The diagram below shows a logic circuit.



(a) Write a Boolean expression for **D**.

.....

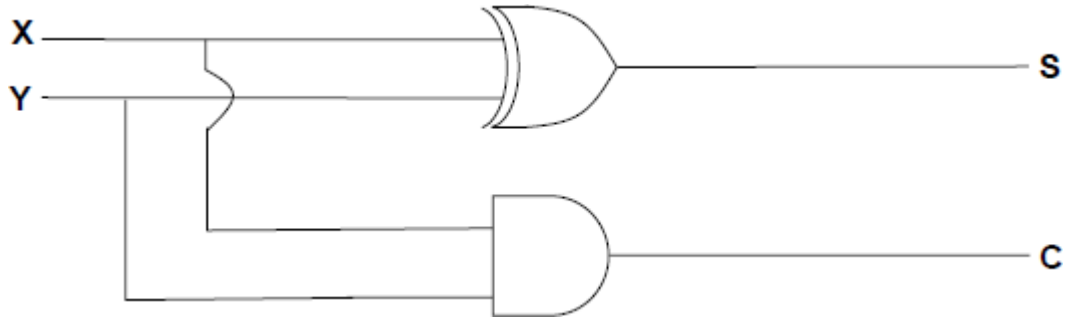
(1)

(b) Write a Boolean expression for **B**.

.....

(1)

(c) The diagram below shows a different logic circuit.



(i) Complete the truth table below for the logic circuit in the diagram above.

Inputs		Outputs	
X	**Y**	**C**	**S**
0	0		
0	1		
1	0		
1	1		

(2)

(ii) What arithmetic function does the logic circuit in the diagram above perform?

.....

(1)

(d) **Without** using a truth table, simplify the Boolean expression below.

$(X + Y) . (X + \overline{Y})$

Show the stages of your working.

.....

.....

.....

.....

.....

.....

.....

.....

.....

.....

.....

(3)

Final answer .....

(1)

(Total 9 marks)

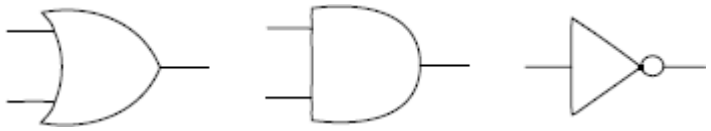
8 (a) Complete the truth tables for the following logic gates.

NAND Gate		
Input X	**Input Y**	**Output Q**
0	0	
0	1	
1	0	
1	1	

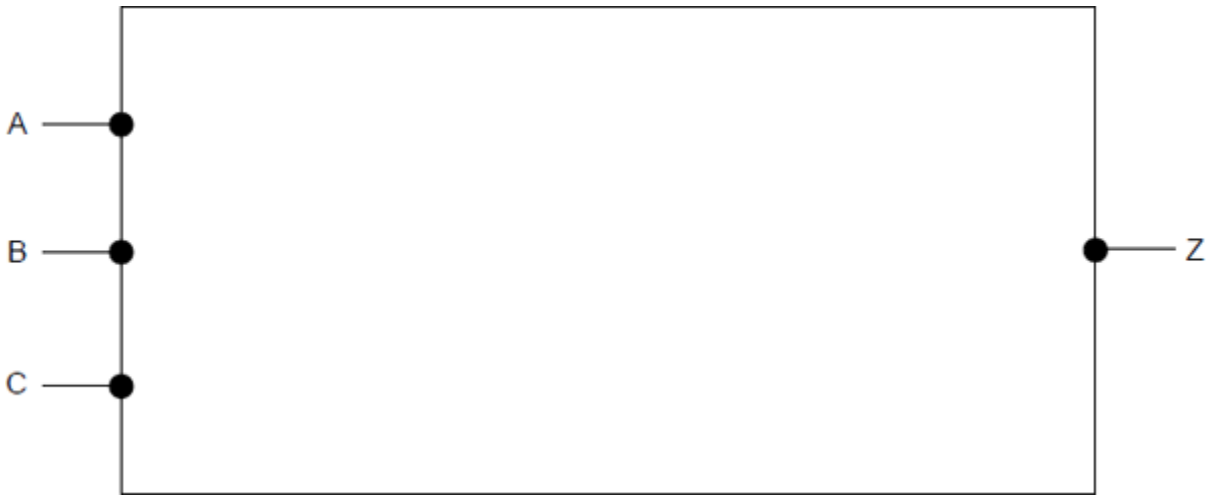
NOR Gate		
Input X	**Input Y**	**Output Q**
0	0	
0	1	
1	0	
1	1	

(2)

(b) Represent the Boolean equation $Z = \overline{A} \cdot \overline{B} + C$ in the form of a logic circuit by drawing a diagram in the space below using the following symbols.



OR AND NOT



(3)

(c) Simplify the Boolean expression below.

$$\overline{(A \cdot B)} + \overline{(A \cdot \overline{\overline{B}})}$$

Show each stage of your working.

.....

.....

.....

.....

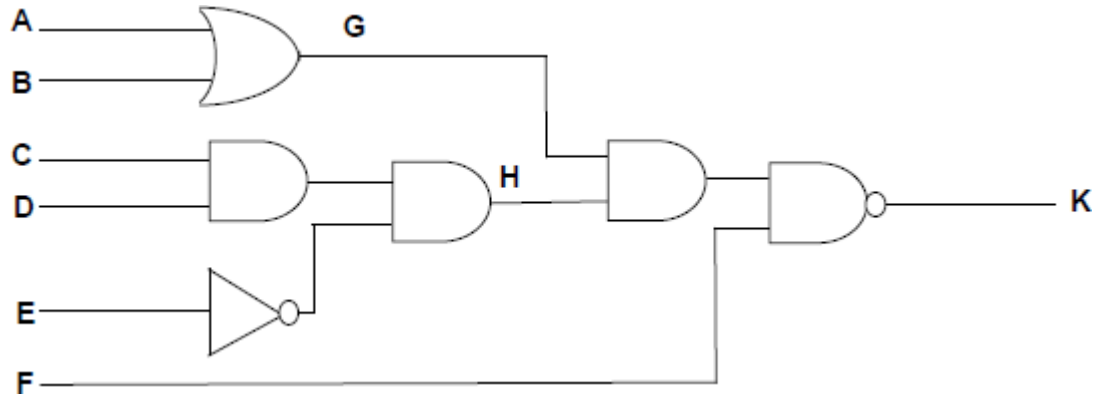
.....

(3)

Final answer .....

(1)
(Total 9 marks)

9 The diagram below shows a logic circuit.



Complete the truth table for the inputs that have been given.

Inputs								
A	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**K**
0	0	1	1	0	0			
0	1	1	1	0	1			
1	0	1	1	1	0			
1	1	1	1	1	1			

(Total 3 marks)

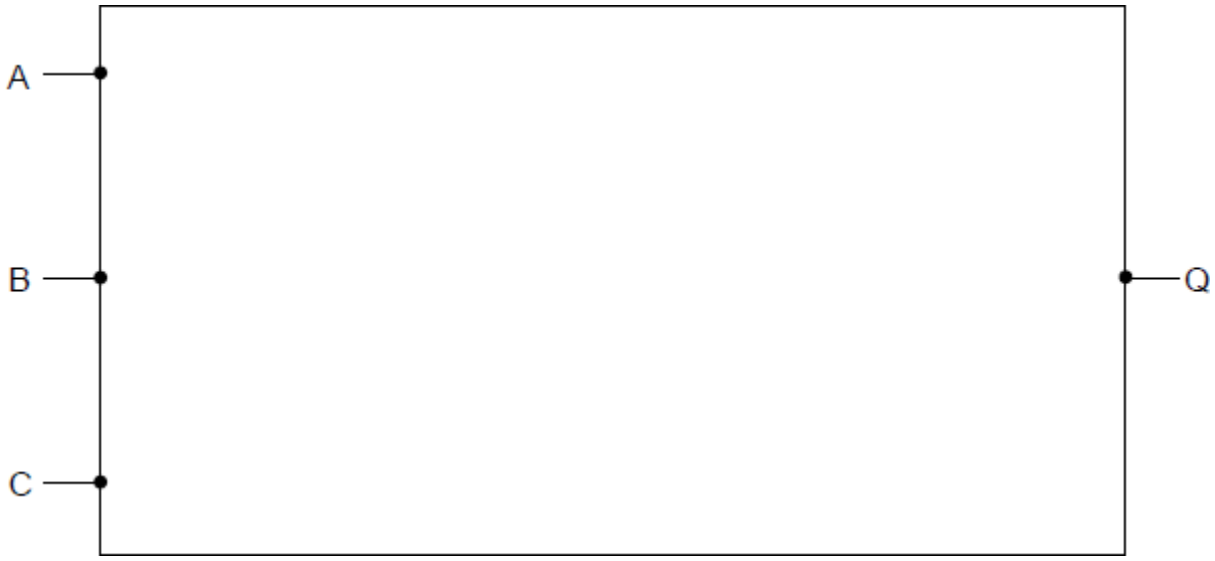
10 (a) Complete the truth tables for the following logic gates.

OR Gate		
Input A	**Input B**	**Output Q**
0	0	
0	1	
1	0	
1	1	

XOR Gate		
Input A	**Input B**	**Output Q**
0	0	
0	1	
1	0	
1	1	

(2)

(b) Represent the Boolean equation $Q = A + B \cdot \overline{C}$. as a logic circuit by drawing a diagram of it in the space below.



(3)

(c) Simplify the Boolean expression:

$$B \cdot (A + \overline{B})$$

Show your working.

.....

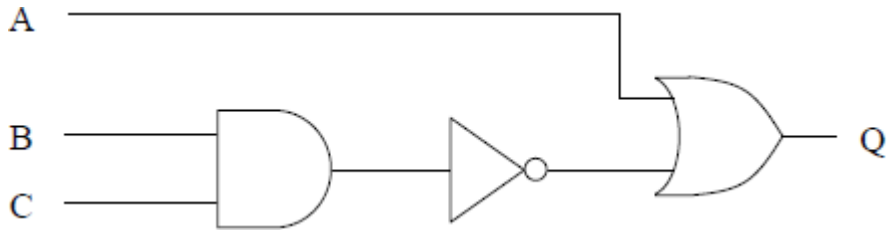
.....

.....

.....

(3)
(Total 8 marks)

11 The figure below shows a logic circuit.



(a) Complete the truth table below for the logic circuit shown in the above figure. Write the correct value of the output Q for each of the listed sets of inputs.

Input A	Input B	Input C	Output Q
1	0	1	
0	1	0	
0	1	1	

(3)

(b) Two of the gates in the circuit shown in the above figure could be replaced by a single gate.

(i) Which **two** gates could be replaced?

.....

(1)

(ii) What single gate would be used instead?

.....

(1)

(c) Why is it an advantage to use as few gates as possible in a logic circuit?

(1)

(Total 6 marks)

12

(a) Look at the truth table below.

Input A	Input B	Output Q
0	0	1
0	1	0
1	0	0
1	1	0

What logic gate does the table represent?

.....

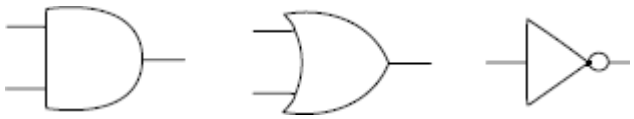
(1)

(b) An interior light in a two-door car is controlled by two switches that the driver can turn on or off and two sensors, one per door.

The switches are named A and B.
The door sensors are named C and D.
The interior light is named L.
If a door is open the output of its sensor is on.
If a door is closed the output of its sensor is off.

- If both switches A and B are off then the light L is always off.
- If switch A is on the light L is always on.
- If switch B is on and switch A is off then:
  - the light L turns on if one or more of the car doors is opened
  - the light L turns off if both of the doors are closed.

The following symbols are used to represent logic gates:



AND OR NOT

(i) Using only AND, OR and NOT gates draw a logic circuit for this system in the box below. You may not need to use all three types of gate.

(3)

(ii) Write a Boolean expression to represent the logic of the interior light system.

.....

(1)

(c) Simplify the Boolean expression below, showing your working.

$$\overline{\overline{A} + \overline{B}} + B \cdot \overline{A}$$

.....

.....

.....

.....

.....

.....

.....

.....

.....

(3)
(Total 8 marks)

13 (a) Complete the truth tables for the following logic gates.

OR gate

Input A	Input B	Output
0	0	
0	1	
1	0	
1	1	

AND gate

Input A	Input B	Output
0	0	
0	1	
1	0	
1	1	

(2)

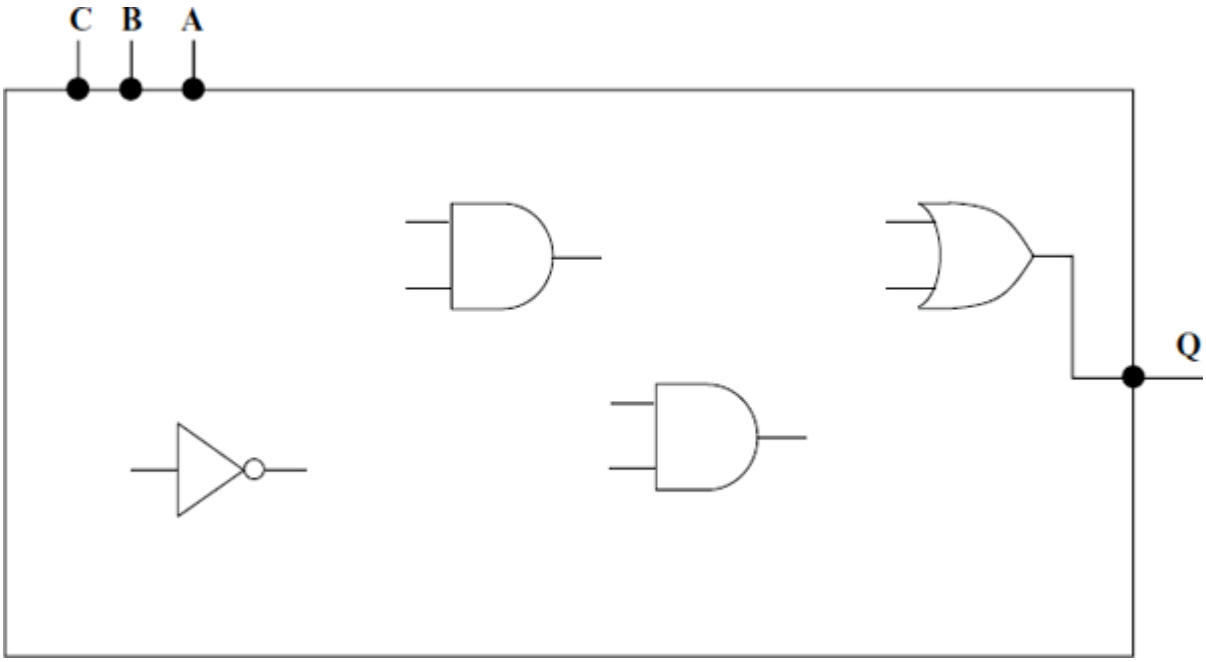
(b) (i) A single output Q is produced from three inputs A, B and C. Output Q is required to be 1 only if inputs A and B are 1, or input C is 1 and input B is 0.

Express this as a Boolean equation.

Q = ...

(2)

(ii) Represent this Boolean equation diagrammatically by completing the logic gate diagram below.



(4)
(Total 8 marks)

14 (a) Complete the table below and draw the symbol for an AND gate in the box.

Truth table for an AND gate

Input A	Input B	Output

AND gate symbol

(2)

(b) Using the laws of Boolean algebra, simplify the following Boolean expression.

A.B. (A + B)

.....

.....

.....

.....

.....

Answer .....

(3)

(c) Using the laws of Boolean algebra, simplify the following Boolean expression.

$(X + Y).(X + \overline{Y})$

.....

.....

.....

.....

.....

Answer .....

(3)
(Total 8 marks)

15 Write the following Boolean expressions in their simplest forms.

(a) $\overline{(\overline{A} . \overline{B})}$

.....

(1)

(b) $B + B . \overline{C}$

.....

(1)

(c) $A . B + A . \overline{B}$

.....

(1)

(d) A . (B+1)

.....

(1)
(Total 4 marks)

16 Simplify the Boolean expression:

$$\overline{A \cdot B} + A$$

Show your working.

.....

.....

.....

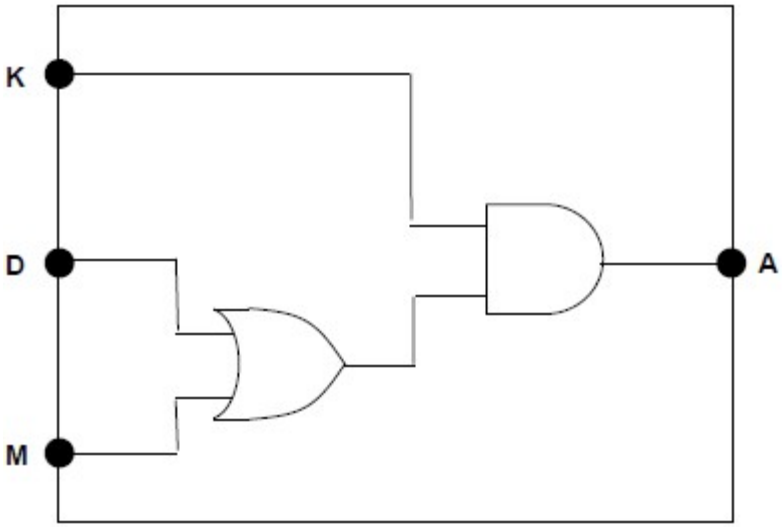
.....

.....

(Total 3 marks)

1

(a) **All marks AO2 (apply)**



1 mark: inputs D and M connected to an OR gate;
1 mark: inputs K and output of OR gate connected to AND gate plus output connected to A;
A a logically equivalent circuit

2

(b) **All marks AO2 (apply)**

A = (D + M) · K
1 mark: D + M somewhere in expression, even if full expression incorrect
1 mark: fully correct expression
A A logically equivalent expression

2

(c) **1 mark for AO1 (understanding), 1 mark for AO2 (application) and 1 mark for AO1 (knowledge)**

AO1 (understanding):1 mark: Flip-flop will store the state of its input / / Flip-flop acts as memory;

AO2 (application):1 mark: Insert into circuit between the output of the OR gate and the AND gate / / after the AND gate;

AO1 (knowledge):1 mark: Clock signal / / trigger / / signal to indicate when the value (of the input) should be stored / read;

3

[7]

2

(a)

Input A	Input B	Output
0	0	1
0	1	1
1	0	1
1	1	0

One mark for having correct values in Output column;

1

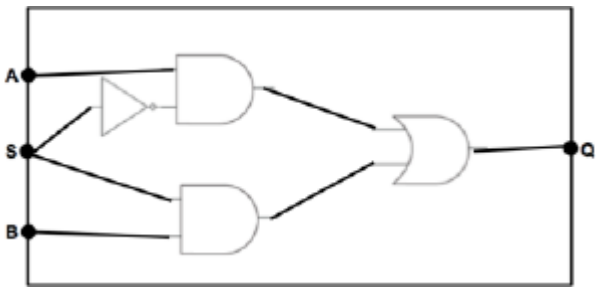
(b) (i)

S	A	B	$\bar{S}$	A.$\bar{S}$	B.S	Q
0	0	0	1	0	0	0
0	0	1	1	0	0	0
0	1	0	1	1	0	1
0	1	1	1	1	0	1
1	0	0	0	0	0	0
1	0	1	0	0	1	1
1	1	0	0	0	0	0
1	1	1	0	0	1	1

Marking:
One mark for the **A.$\bar{S}$** column being correct;
One mark for the **B.S** column being correct;
The final **Q** column should follow through from the previous two columns as an OR statement;

3

(ii)



One mark for NOT gate with input from S;
A just a circle on AND gate input from S

One mark for AND gate with input from NOT S and A;
A if no NOT gate from S

One mark for AND gate with input from B and S;

One mark for output from AND gates going into OR gate with output connect to Q;

4

(iii) A multiplexor selects one of several input lines / wires and forwards / duplicates the Boolean value on this one line onto a single line / wire;

If S is 1 then input B is output otherwise input A is output // if S is 0 then input A is output otherwise input B is output;

Note:
1 can be mapped to on / true / high
0 can be mapped to off / false / low

MAX 1

[9]

3

(a) OR gate

Input A	Input B	Output
0	0	**0**
0	1	**1**
1	0	**1**
1	1	**1**

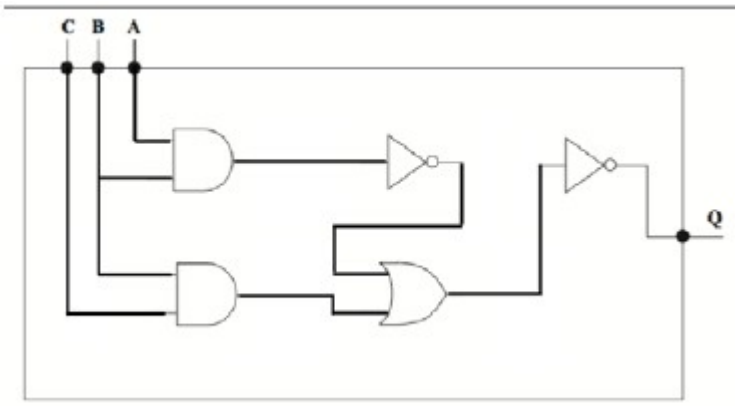
NAND gate

Input A	Input B	Output
0	0	**1**
0	1	**1**
1	0	**1**
1	1	**0**

1 mark for correct output OR gate;
1 mark for correct output NAND gate;

2

(b)



1 mark for inputs A and B connected to AND gate;
1 mark for inputs B and C connected to AND gate;
1 mark for output of AND (A,B input) as only connection going to NOT gate;
1 mark for output of NOT gate plus the AND gate (B,C input) going to OR gate;
1 mark OR gate as only connection going to NOT gate and output only connection to Q;

5

(c) **MAX 2 if working out is not logically sound**

Example 1:

$\overline{\overline{\mathbf{A}} + \overline{\mathbf{B}}} + \mathbf{B}.\overline{\mathbf{A}}$

$\mathbf{A}.\mathbf{B} + \mathbf{B}.\overline{\mathbf{A}}$
Having applied De Morgan's correctly;

$\mathbf{B}.(\mathbf{A} + \overline{\mathbf{A}})$
Having factorised;

Final answer: **B** ;

Example 2:

$\overline{\overline{\mathbf{A}} + \overline{\mathbf{B}}} + \mathbf{B}.\overline{\mathbf{A}}$

$\overline{(\overline{\mathbf{A}} + \overline{\mathbf{B}}).(\overline{\mathbf{B}} + \mathbf{A})}$
Having applied De Morgan's correctly;

$\overline{\overline{\mathbf{A}}.\overline{\mathbf{B}} + \overline{\mathbf{A}}.\mathbf{A} + \overline{\mathbf{B}}.\overline{\mathbf{B}} + \overline{\mathbf{B}}.\mathbf{A}}$
Expanded bracket;

$\overline{\overline{\mathbf{A}}.\overline{\mathbf{B}} + \mathbf{0} + \overline{\mathbf{B}} + \overline{B}.A}$
Simplified elements

Having used C + C.D = C to simplify

$\overline{\overline{\mathbf{B}}}$
Having used C + C.D = C to simplify again

Final answer: B ;

Truth Table Answer

A	**B**	$\overline{\overline{\mathbf{A}} + \overline{\mathbf{B}}}$	$\mathbf{B}.\overline{\mathbf{A}}$	$\overline{\overline{\mathbf{A}} + \overline{\mathbf{B}}} + \mathbf{B}.\overline{\mathbf{A}}$
0	0	0	0	0
0	1	0	1	1
1	0	0	0	0
1	1	1	0	1
		X	**Y**	**Z**

1 mark for both columns marked X and Y above; (column X could be labelled **A.B**)
1 mark for final column Z;
1 mark for final answer: B;

3

[10]

4

(a) AND;
NOR;
XOR; **A** EXOR // EOR // NEQ // exclusive OR;

3

(b) (i) B

1

(ii) B

1

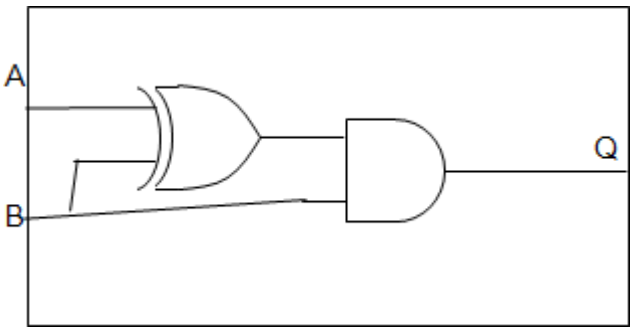
(iii) 0;;

Award 1 mark if De Morgan's has been applied once correctly but candidate does not end up simplifying to 0

Example: $\overline{B + (\bar{A} + \bar{B})}$
Example: $\bar{B} . (A . B)$

2

(c)



Inputs A and B connected to an XOR gate;

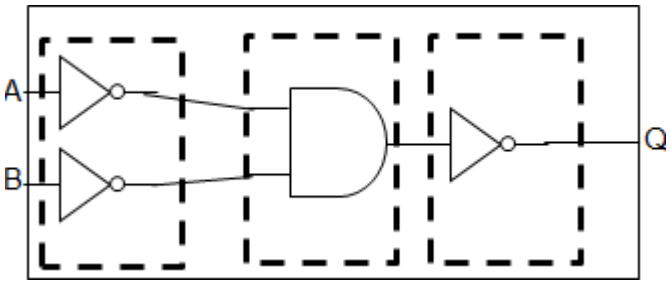
Input from B and output of XOR gate connected to an AND gate with output going to Q;

2

[9]

5

(a)



1 mark – logic of first part satisfies NOT A, NOT B;
1 mark – inputs into an AND gate;
1 mark – output from AND gate passes through a NOT gate and connected to Q;

3

(b)

A	B	A + B
0	0	0
0	1	1
1	0	1
1	1	1

1 mark for correct A + B column;

A	B	$\overline{A}$	$\overline{B}$	$\overline{A}.\overline{B}$	$\overline{\overline{A}.\overline{B}}$
0	0	1	1	1	0
0	1	1	0	0	1
1	0	0	1	0	1
1	1	0	0	0	1

1 mark for columns $\overline{A}$ and $\overline{B}$ column being correct;
1 mark for $\overline{\overline{A}.\overline{B}}$ column being correct;
1 mark for $\overline{A}.\overline{B}$ column being correct;

Note: Can follow through into $\overline{A}.\overline{B}$ column from previous two

4

(c) De Morgan's (law);

1

(d) **Mark allocation:**
One mark for taking either A, NOT C or A AND NOT C outside of brackets to produce a correct expression;
One mark for eliminating B in a valid way;
One mark for correct final answer;

Example One:
$A.B.\overline{C} + A.\overline{C}$

$A\ (B.\overline{C} + \overline{C})$ - taking A outside of brackets;

$A\ (\overline{C}(B + 1))$ $(B + 1) = 1$
Simplifying to remove B using $B + 1 = 1$;

$B.\overline{C} + \overline{C} = \overline{C}$
Simplifying to remove B using $B.\overline{C} + \overline{C} = \overline{C}$;

A $A(\overline{C}\ (B + 1)) \longrightarrow A.\overline{C}$;

Final answer $A.\overline{C}$

Example Two:

$A.B.\overline{C} + A.\overline{C}$

$A.\overline{C}(B + 1)$ – taking outside of brackets;

$(B + 1) = 1$; - simplifying to remove B

A $A.\overline{C}(B + 1) \longrightarrow A.\overline{C}$

Final answer $A.\overline{C}$

Truth Table Method

A	B	C		$A.\overline{C}$	$A.B.\overline{C} + A.\overline{C}$
0	0	0		0	0
0	0	1		0	0
0	1	0		0	0
0	1	1		0	0
1	0	0		1	1
1	0	1		0	0
1	1	0		1	1
1	1	1		0	0

(student answer may have more columns than this)

A mark for having correct column for A.B.$\overline{C}$ + A.$\overline{C}$;
A mark for having correct column for A.$\overline{C}$;
Final answer A.$\overline{C}$

3

[11]

6 (a)

AND Gate		
Input X	**Input X**	**Output Q**
0	0	0
0	1	0
1	0	0
1	1	1

XOR Gate		
Input X	**Input X**	**Output Q**
0	0	0
0	1	1
1	0	1
1	1	0

1 mark for each of the output columns

2

(b) (i) $(L \oplus R).\ \overline{U}$

[Brackets are not necessary]

1 mark for use of correct operands (L,R,U);
1 mark for use of XOR with L,R;
1 mark for NOT U anded with other part;

alternative: $(L + R).\ (\overline{L.R}).\overline{U}$

1 mark for use of correct operands (L,R,U);
1 mark for alternative XOR expression;
1 mark for AND NOT U;

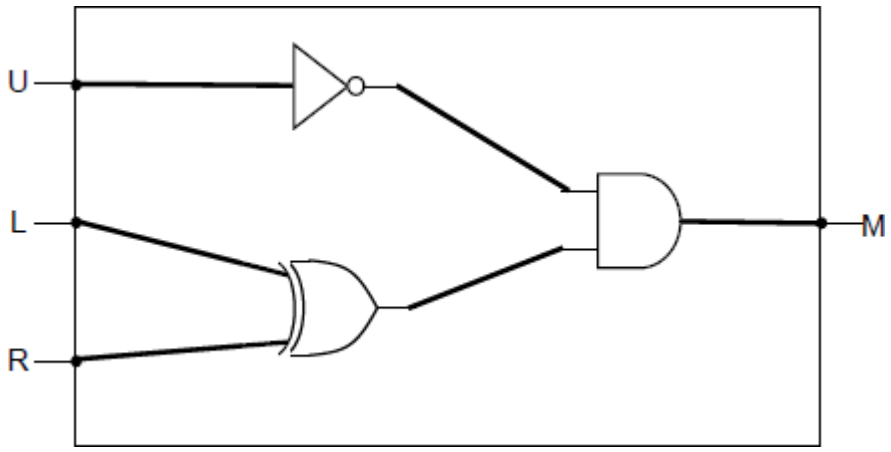
alternative: $(\ L.\ \overline{R} + \overline{L}.R).\ \overline{U}$

1 mark for use of correct operands (L,R,U);
1 mark for alternative XOR expression;
1 mark for AND NOT U;

Acceptable notation for symbols
~ for NOT
X.Y allow X AND Y, XэY,X)Y, XY
*X+Y allow X OR Y, X(Y, X*Y*

3

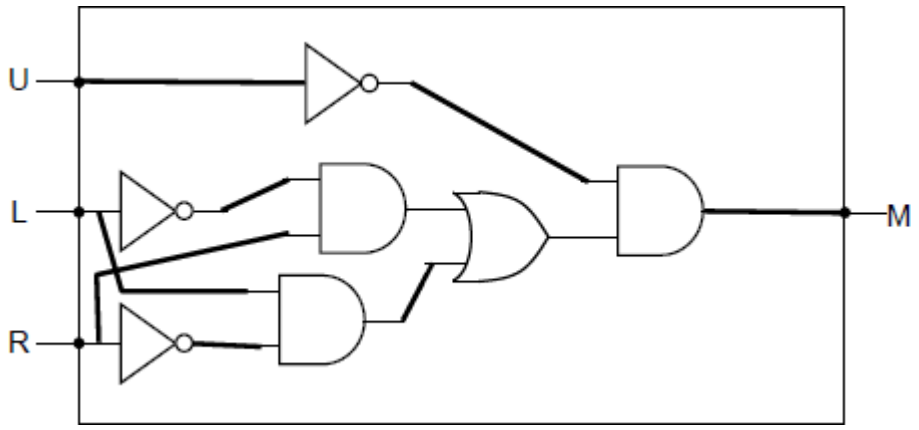
(ii)



L, R connected to XOR gate;
U connected to NOT gate;
Output of a two input AND gate connected to M;

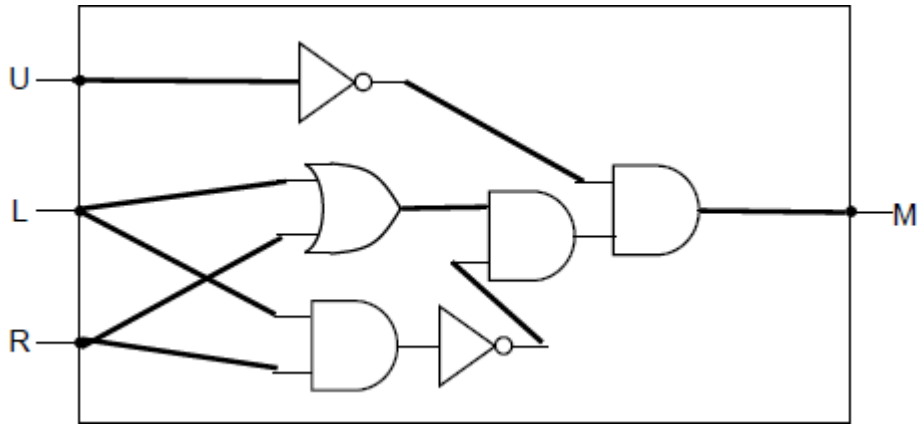
Max 2 if circuit does not reflect the correct logic

Alternative :



U connected to NOT gate;
Correct gates used for L and R before last AND gate;
Output of a two input AND gate connected to M;

Alternative :



Marked as above alternative.

3

(c) **Solution 1:**

$Q = \overline{\overline{A}.(B.A)}$ [Application of De Morgan's Law – **1 mark**]
$Q = A.B.A$ [allow simplification of double nots at same time]
[Simplification of A.A to A –**1 mark**]
$Q = A.B$ [Correct solution – **1 mark**]

Solution 2:

$Q = \overline{A} + (\overline{\overline{B} + \overline{A}})$ [Application of De Morgan's Law – **1 mark**]

$Q = \overline{\overline{A} + \overline{B} + \overline{A}}$ [allow simplification of double nots at same time]

$Q = \overline{\overline{A} + \overline{B}}$ [Simplification of NOT A OR NOT A to NOT A – **1 mark**]

$Q = A.B$ [De Morgan's again to correct solution – **1 mark**]

1 mark for De Morgan;
1 mark for simplification;
1 mark for final answer;
Other notations as for section (b)

No working marks for truth table solution (asked to use De Morgan's in question)

3

[11]

7

(a) X $\oplus$ Y;

$X.\overline{Y} + \overline{X}.Y$

A alternative notations:
X XOR Y
X EOR Y
X AND NOT Y OR NOT X AND Y

Acceptable notation for symbols :
For X.Y allow X∧Y, X∩Y, XY
For X+Y allow XvY,XUY
For X allow ~X

1

(b) $X.\overline{Y}$;

A alternative notations : X AND NOT Y;

1

(c) (i)

Inputs		Outputs	
X	**Y**	**C**	**S**
0	0	**0**	**0**
0	1	**0**	**1**
1	0	**0**	**1**
1	1	**1**	**0**

One mark for C column;
One mark for S column;

2

(ii) Addition // adder;
A sum;

1

(d) $(X+Y).(X+\overline{Y})$ *[Fully expanding brackets – 1 mark]*

$X.X+X.\overline{Y}+Y.X+Y.\overline{Y}$ *[Recognising X.X = X OR Y.$\overline{Y}$ = 0 –1 mark]*

$X+X.\overline{Y}+Y.X+0$ *[Taking X outside brackets – 1 mark]*

$X(1+\overline{Y}+Y)$ OR $X+X(\overline{Y}+Y)$ *X[Final Answer, 1 mark]*

Alternative Answer : (Distributive)

$(X+Y).(X+\overline{Y})=X+(Y.\overline{Y})$ *[Use of distributive law – 1 mark]*

$X+(Y.\overline{Y})=X+0$ *[Recognising Y .$\overline{Y}$ = 0 – 1 mark]*

X + 0 = X *[1 mark]*

X *[Final Answer, 1 mark]*

Alternative Answer : (De Morgan's)

$\overline{\overline{X+Y}+\overline{X+\overline{Y}}}=Q$ *[Use of De Morgan's – 1 mark]*

$\overline{X+Y}+\overline{X+\overline{Y}}=\overline{Q}$

$\overline{\overline{X}.+\overline{Y}}+\overline{\overline{X}.+\overline{\overline{Y}}}=\overline{Q}$ *[Two further applications of De Morgan's]*

$\overline{X}.\overline{Y}+\overline{X}.Y=\overline{Q}$ *[Taking X outside brackets – 1 mark]*

$\overline{X}.(\overline{Y}+Y)=\overline{Q}$ *[Recognising ~Y + Y = 1 – 1 mark]*

$\overline{X}.1=\overline{Q}$ *[Recognising X.1=X – 1 mark]*

$\overline{X}=\overline{Q}$

$X=Q$ *[Final answer, 1 mark]*

Max 3 for working/method;
1 for final answer
X on own with no working gains 1 mark.

Max 4

[9]

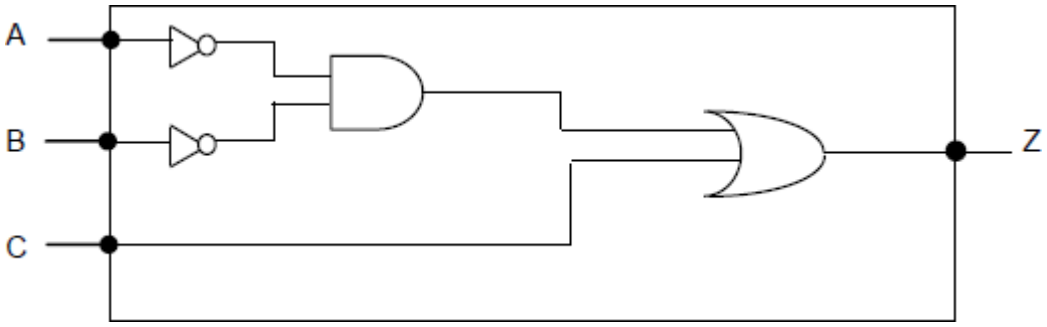
8

(a)

NAND	NOR
1	1
1	0
1	0
0;	0;

2

(b)



1 mark for NOT gates on both A and B;
1 mark for AND with inputs from $\overline{A}$ *and* $\overline{B}$*;*
A inputs from A and B
1 mark for OR gate with inputs from AND gate output and C and output connected to Z;

3

(c) $\overline{(A.B)}+\overline{(A.\overline{B})}$

$(\overline{A}+\overline{B})+(\overline{A}+B)$; ; *2 marks – 1 each for De Morgans rule for each side of the central OR (award the mark for right hand expression, even if double NOT over B is not cancelled)*

$\overline{A}+\overline{B}+B$ Recognising NOT A OR NOT A is NOT A, and producing a correct expression

$\overline{A}$*+1; Recognising B or NOT B is 1*

Final answer 1 ;

Alternative answer

$\overline{\overline{(A.B)}.\overline{(A.B)}}$; Application of De Morgan's to entire expression

$\overline{(A.B).\overline{(A.\overline{B})}}$; Cancellation of NOTs; 1 mark – De Morgans on entire expression

$\overline{A.B.\ B}$ Recognising A and A is A

$\overline{A.0}$ Recognising B ANDed with its complement is 0

$\overline{0;}$ Recognising 0 AND anything is 0

Final answer 1 ;

Note: Marks can be awarded for the skills above if seen but Max 3 (out of 4) for whole question if working has errors in it

A T, True for 1 and F, False for 0
A alternative notations :

- For X.Y allow X AND Y, X ∧ Y,X∩Y, XY
- For X+Y allow X OR Y, X v Y, X U Y
- For $\overline{X}$ allow NOT X, ¬X

Or by truth table M = marking point

			M		M	M	M	M
A	B	A.B	$\overline{A.B}$	$\overline{B}$	$A.\overline{B}$	$\overline{A.\overline{B}}$	$\overline{A.B}$ + $\overline{A.\overline{B}}$	1
0	0	0	1	1	0	1	1	
0	1	0	1	0	0	1	1	
1	0	0	1	1	1	0	1	
1	1	1	0	0	0	1	1	

Max 3 for stages, 1 for final answer

4

[9]

9

G	H	K
0	1	1
1	1	0
1	0	1
1	0	1
;	;	;

1 mark for each correct column

[3]

10

(a)

OR Gate		
Input A	**Input B**	**Output Q**
0	0	**0**
0	1	**1**
1	0	**1**
1	1	**1**

1 mark

XOR Gate		
Input A	**Input B**	**Output Q**
0	0	**0**
0	1	**1**
1	0	**1**
1	1	**0**

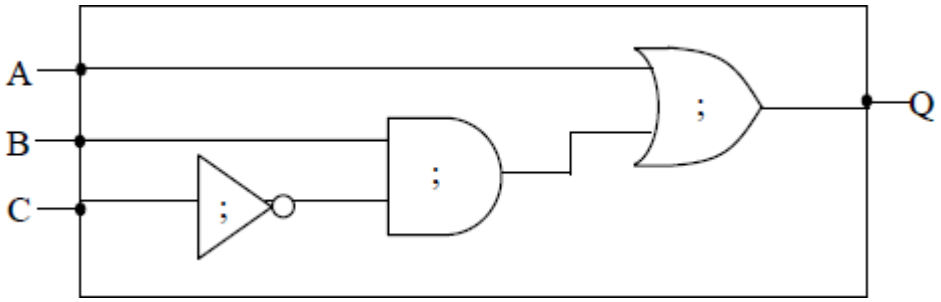
1 mark

1 mark for each correct output column

A True for 1, False for 0

2

(b)



1 mark for NOT gate correctly linked to input C;
1 mark for AND gate correctly linked to B and $\overline{C}$ *as input;*
A if AND gate linked directly to C
1 mark for OR gate with inputs from A and the output of an AND gate and output connected to Q;

3

(c) **Algebraic solution:**

B.(A + $\overline{B}$)
B.A + B. $\overline{B}$ [*1 mark for expansion of brackets*]
B.A + 0 [*1 mark for identifying that B.*$\overline{B}$ *= 0*]
B.A [*1 mark for correct answer*]

Truth table solution:

		X	Y	Z
A	B	$\overline{B}$	$A+\overline{B}$	$B\cdot(A+\overline{B})$
0	0	1	1	0
0	1	0	0	0
1	0	1	1	0
1	1	0	1	1

1 mark for both columns X and Y correct
1 mark for column Z correct
1 mark for correct answer (B.A)

Any other method:
If student has used any other method to arrive at correct answer then award marks as follows:
1 mark for correct answer, no working out
2 marks for correct answer with working out, not all steps shown.
3 marks for correct answer with all steps of working out shown.

A True for 1, False for 0
A alternative notations :

- For X.Y allow X AND Y, X ∧ Y ,X∩Y, XY
- For X+Y allow X OR Y, X ∨ Y , XUY
- For $\overline{X}$ allow NOT X, ¬X

3

[8]

11

(a) 1; **A** True
1; **A** True
0; **A** False

3

(b) (i) AND and NOT

1

(ii) NAND // NAND gate
R NOT AND

1

(c) Minimise cost of production;
Reduce propagation delay//speed up processing;
Minimise heat generated;
Reduce power consumption;
NE simpler to produce/makes circuit simpler
NE reduce number of gates in chip

1

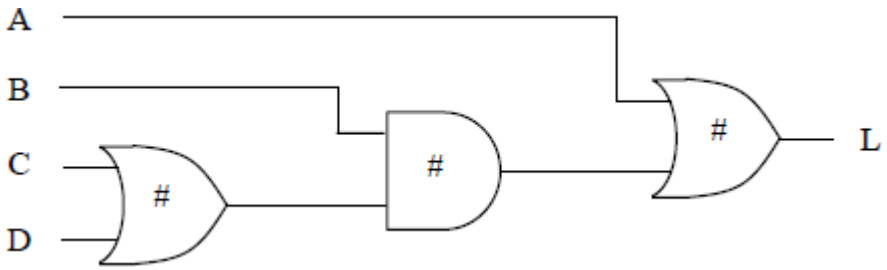
[6]

12

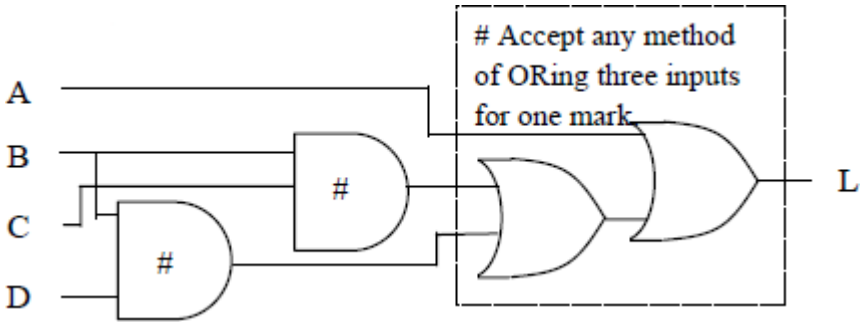
(a) NOR (Gate)
I case of answer i.e. nor is allowed

1

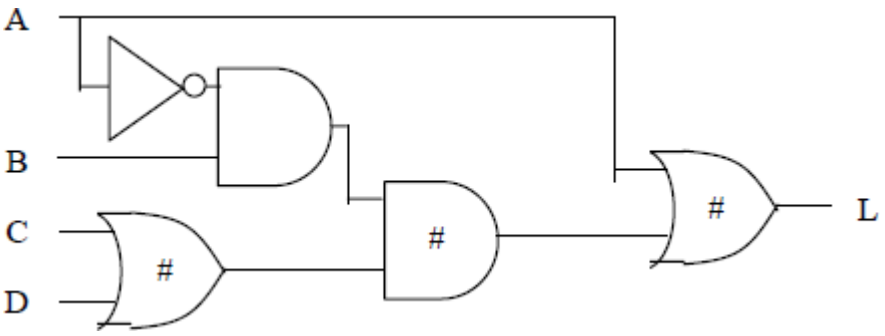
(b) (i) Solution 1:



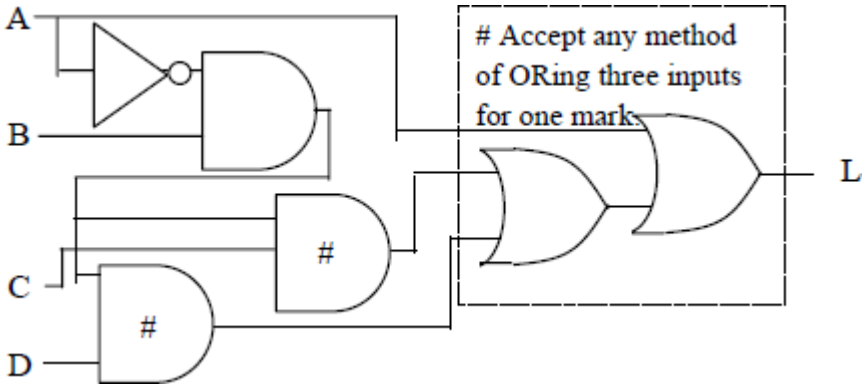
Solution 2:



Solution 3 (solution 1 plus check for A off):



Solution 4 (solution 2 plus check for A off):



1 mark for each correctly linked gate that is marked with a #

A 3-input OR gate
P1 for any unnecessary gates in a solution that would otherwise get 3 marks.
P1 for any solution that would not correctly implement the logic but would otherwise get 3 marks.

Mark from left to right until first mistake encountered then from right to left. When marking left to right award 1 mark for each gate correctly connected to its inputs. When marking right to left award 1 mark for each gate correctly connected to its output.

3

(ii) A + B.(C+ D)
A + B.C+ B.D
A + $\overline{A}$.B. (C+ D)
A + $\overline{A}$.B.C+ $\overline{A}$.B.D

A Insertion of extra brackets that do not affect logic of expression
Note: Expression does not need to match diagram drawn in (i).
A alternative notations :

- For X.Y allow X AND Y, X $\wedge$ Y , X $\cap$ Y, XY
- For X+Y allow X OR Y, X $\vee$ Y , X $\cup$ Y
- For $\overline{X}$ allow NOT X, $\neg$X

1

(c) **Algebraic Solution:**

$\overline{\overline{A} + \overline{B}} + B.\overline{A}$ [Application of DeMorgan's Law *1 mark*]

$A.B + B.\overline{A}$ [Common term B taken out *1 mark*]

$B.(A + \overline{A})$ // B.1

B [Correct answer *1 mark*]

A alternative notations :

- For X.Y allow X AND Y, X ∧Y , X ∩ Y, XY
- For X+Y allow X OR Y, X ∨ Y , X∪Y
- For X allow NOT X, ¬X

Truth Table Solution:

				X	**Y**	**Z**
A	B	$\overline{A}$	$\overline{B}$	$\overline{\overline{A}+\overline{B}}$	$B \cdot \overline{A}$	$\overline{\overline{A}+\overline{B}}+B \cdot \overline{A}$
0	0	1	1	0	0	0
0	1	1	0	0	1	1
1	0	0	1	0	0	0
1	1	0	0	1	0	1

1 mark for both columns X and Y correct
1 mark for column Z correct
1 mark for correct answer (B)

A Rightmost column labelled as L or Q

3

[8]

13

(a)

OR

Input A	Input B	Output
0	0	**0**
0	1	**1**
1	0	**1**
1	1	**1**

AND

Input A	Input B	Output
0	0	**0**
0	1	**0**
1	0	**0**
1	1	**1**

1 mark per correct table

2

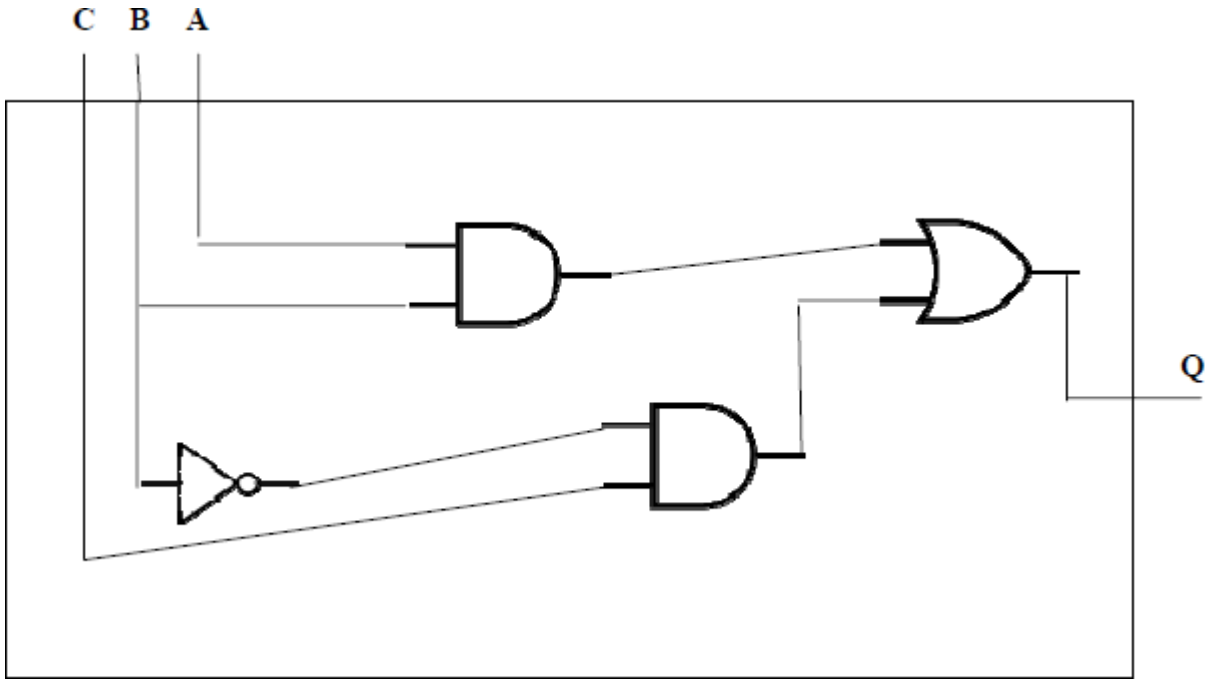
(b) (i) $Q = A.B + C.\overline{B}$

1 mark for A.B or for $C.\overline{B}$
2 marks for $A.B + C.\overline{B}$

A AND instead of .
A OR instead of +

2

(ii) *1 mark for each gate with correct inputs;;;;*
Allow two lines from B



4

[8]

14 (a) **Marks are for AO1 (knowledge)**

A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

1 mark: Table completed correctly;
1 mark: AND gate symbol drawn;

2

(b) **Marks are for AO2 (apply)**

A.B.(A + B)
A.B.A + A.B.B ; [expansion of brackets]
B.A + A.B ; [use of A.A = A]
A.B ; [use of A + A = A]

1 mark: Final answer: A.B;
Max 2 for working

3

(c) (**Marks are for AO2 (apply)**

X + Y).(X + NOT Y)
XX + X(NOT Y) + XY + Y(NOT Y) ; [expansion of brackets]
X + X(NOT Y) + XY ; [use of X.X = X or use of Y(NOT Y) = 0]
X (1 + NOT Y + Y) ; [use of 1 + X = 1]

1 mark: Final answer - X;
Max 2 for working

3

[8]

15

$\overline{\overline{A}.\overline{B}}$ becomes A + B ;
A (A+B);
A A OR B;
B+ B.$\overline{C}$ becomes B ;
A B+ A. $\overline{B}$ becomes A ;
A (B+1) becomes A ;

1 mark for each

[4]

16

Algebraic Solution:

Method 1	**Method 2**
$\overline{A.B}$ + A $= \overline{A} + \overline{B} + A$ $= 1 + \overline{B}$ = 1	$\overline{A.B}$ + A $= \overline{A.B.\overline{A}}$ $= \overline{0.B}$ $= \overline{0}$ = 1

1 mark for an application of a DeMorgan's law

1 mark for realisation that A + $\overline{A}$ + $\overline{B}$ = 1 + $\overline{B}$ or $\overline{0.B}$ = $\overline{0}$ (must be written in method, not just inferred that student has done this if arrives at correct answer)
1 mark for correct answer

Truth table solution:

		X	Y	Z
A	B	$A \cdot B$	$\overline{A \cdot B}$	$\overline{A \cdot B} + A$
0	0	0	1	1
0	1	0	1	1
1	0	0	1	1
1	1	1	0	1

1 mark for column Y correct
1 mark for column Z correct
1 mark for correct answer

Any other method:
If student has used any other method to arrive <u>at correct answer</u> then award marks as follows:
1 mark for correct answer, no working out
2 marks for correct answer with working out, not all steps shown.
3 marks for correct answer with all steps of working out shown.

A True for 1, False for 0
A alternative notations :

- For X.Y allow X AND Y, X ∧Y ,X∩Y, XY
- For X+Y allow X OR Y, X ∨Y , X∪Y
- For $\overline{X}$ allow NOT X, ¬X

[3]